LADDER ANALYSIS PROGRAM

FOR THE HP-41C

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AS-49-34

STK#484796

"BLAP": BACKWARDS LADDER ANALYSIS PROGRAM

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ONE OF THE SIMPLEST WAYS TO ANALYZE A LADDER CIRCUIT IS TO ASSUME AN OUTPUT CURRENT; THEN WORK BACKWARDS THROUGH THE NETWORK OBTAINING ALL VOLTAGES AND CURRENTS IN TERMS OF THE ASSUMED OUTPUT CURRENT. FOR A LINEAR NETWORK, GAIN AND IMPEDANCE THROUGHOUT THE CIRCUIT ARE INDEPENDENT OF ACTUAL CURRENT AND VOLTAGE LEVELS AND THE RESPONSE (ALL VOLTAGES AND CURRENTS) DUE TO ONE VALUE OF EXCITATION MAY BE LINEARLY SCALED TO ANOTHER VALUE OF EXCITATION - FOR EXAMPLE YOU MIGHT WANT TO KNOW ALL VOLTAGES AND CURRENTS WITHIN A CIRCUIT FOR A SPECIFIC INPUT POWER IN ORDER TO DETERMINE THE VOLTAGE AND CURRENT RATINGS OF ALL THE COMPONENTS.

"BLAP" IS A COLLECTION OF SUBROUTINES FOR THE HP-41C WHICH EMPLOYS THE "BACKWARDS" ALGORITHM. THE LOAD CURRENT IS ASSUMED 1.0+J0 AMPERES FOR CONVENIENCE. THIS MAKES THE LOAD VOLTAGE RL VOLTS FOR RESISITIVE LOAD RL AND THE LOAD POWER IS RL WATTS. WORKING BACK TOWARD THE GENERATOR; IF A SERIES IMPEDANCE IS ENCOUNTERED THE CURRENT IS UNCHANGED BUT THE VOLTAGE IS INCREASED BY THE DROP ACROSS THE SERIES IMPEDANCE (V=V+I*ZS). IF A PARALLEL ADMITTANCE IS ENCOUNTERED THE VOLTAGE IS UNCHANGED BUT THE CURRENT IS INCREASED BY THE CURRENT FLOWING THROUGH THE SHUNT ADMITTANCE (I=I+YP*V). A LIBRARY OF 28 SERIES/PARALLEL TYPE ELEMENTS IS AVAILABLE (ALL SIMPLE SERIES/PARALLEL RLC COMBINATIONS, OPEN AND SHORTED TRANSMISSION LINE STUBS, AND SERIES AND SHUNT IMPEDANCES). TWO-PORT ELEMENTS MAY ALSO BE INCLUDED IN A LADDER CIRCUIT. FOUR TWO-PORT ELEMENTS ARE PROVIDED:

GB	RESISTIVE FEEDBACK GAIN BLOCK
BG	"BACKWARDS" GAIN BLOCK
TL	TRANSMISSION LINE
TF	IDEAL TRANSFORMER.

THE GAIN BLOCK IS A REASONABLE APPROXIMATION OF A SINGLE TRANSISTOR BROADBAND RESISTIVE FEEDBACK AMPLIFIER WHICH IS COMMONLY EMPLOYED IN MODERN CIRCUIT DESIGN (AVANTEK, OPTIMAX, W-J, ANZAC, ETC. AMPLIFIERS) AND INCLUDES THE COUPLING FROM LOAD TO SOURCE DUE TO THE INTENTIONAL FEEDBACK. BG IS THE SAME GAIN BLOCK IN THE REVERSE DIRECTION WHICH ALLOWS ANALYSIS IN EITHER DIRECTION OF ANY LADDER CIRCUIT, EVEN ONE INCLUDING AMPLIFIERS.

ALL ELEMENT SUBROUTINES ARE GIVEN GLOBAL LABELS SO THAT THEY MAY BE CALLED BY A SEPARATE PROGRAM WHICH DESCRIBES THE CIRCUIT. OTHER ELEMENT SUBROUTINES MAY BE ADDED TO "BLAP" -OR UNUSED ONES MAY BE DELETED. THE SUBROUTINE MUST COMPUTE THE INPUT CURRENT AND VOLTAGE IN TERMS OF THE "KNOWN" OUTPUT CURRENT AND VOLTAGE FOR THE ELEMENT BEING MODELED. A BRIEF STUDY OF THE REGISTER USAGE, THE APPENDIX, AND THE PROGRAM LISTING OF SOME OF THE SUBROUTINES USED SHOULD ENABLE THE USER TO GENERATE HIS OWN NEW ELEMENTS.

SIX "COMPUTE AND PRINT" COMMANDS ARE AVAIABLE IN THE BLAP PROGRAM:

"RL" INITIALIZES LOAD AND "AVIEWS" FREQUENCY
"RG" COMPUTES AND "AVIEWS" GAIN
"S" COMPUTES AND "AVIEWS" FORWARD AND INPUT "S" PARAMETERS (SF AND SI) IN DB
"Z" COMPUTES AND "AVIEWS" Z=V/I AT ANY POINT
"VP" "AVIEWS" V AT ANY POINT
"IS" "AVIEWS" I AT ANY POINT

EXCEPT FOR "RL" WHICH INITIALIZES THE CIRCUIT (AND IS THE FIRST COMMAND USUALLY EXECUTED), THE V,I DATA IS NOT DISTURBED BY ANY OF THE COMMANDS SO THESE MAY BE EXECUTED ANYWHERE WITHIN THE CIRCUIT. "RG" OR "S" WILL NORMALLY BE THE LAST COMMAND EXECUTED. IN ADDITION TO THE SIX COMMANDS ABOVE, REGISTER USAGE IN BLAP IS COMPATIBLE WITH "PRPLOT" IN THE PRINTER ROM MAKING IT EASY TO PLOT ANY DESIRED CIRCUIT RESPONSE. "PRPLOT" SUPPLIES THE FREQUENCY TO THE CIRCUIT DESCRIPTION PROGRAM WHICH IN TURN RETURNS THE COMPUTED PARAMETER TO "PRPLOT".

USING BLAP

"BLAP" COMMANDS MAY BE MANUALLY EXECUTED TO ANALYZE A GIVEN CIRCUIT AT A SINGLE FREQUENCY; HOWEVER MOST OF THE TIME THE COMMANDS WILL BE STORED IN A PROGRAM IN ORDER TO "SWEEP" THE SELECTED RESPONSE VERSUS FREQUENCY. THE PRESENT ANALYSIS FREQUENCY -IN GHZ- MUST BE STORED IN REGISTER 08 SO THE CIRCUIT DESCRIPTION PROGRAM WILL USUALLY BE CONTAINED WITHIN A LOOP WHICH INCREMENTS R08 EITHER LINEARLY (ADDITIVE INCREMENTS) OR LOGARITHMICALLY (MULTIPLICATIVE INCREMENTS). "PRPLOT" AUTOMATICALLY PROVIDES A LINEARLY INCREMENTED FREQUENCY (X) LOOP. "PRPLOT" CAN BE MADE TO PROVIDE MULTIPLICATVE INCREMENTS BY INITIALLY SPECIFYING A SMALL NON ZERO "X INCREMENT" THEN MULTIPLY R06 BY THE DESIRED INCREMENT IN THE CIRCUIT DESCRIPTION PROGRAM (R06 IS "PRPLOT" X). R17 CONTENTS ARE TACKED ONTO THE DISPLAY NAME FOR "Z", "VP", OR "IS" TO KEEP TRACK OF THE OUTPUT DATA. USUALLY START WITH 0 IN R17 AT LOAD END AND INCREMENT R17 BY ONE FOR EACH NEW ELEMENT ADDED. BEGIN THE PROGRAM WITH AN "RL" LOAD INITIALIZE COMMAND THEN WORK TOWARD THE GENERATOR USING THE ELEMENT COMMANDS TO DESCRIBE THE CIRCUIT - YOU MAY ASSIGN OFTEN-USED COMMANDS AND ELEMENTS TO USER KEYS TO SAVE TIME. OUTPUT COMMANDS MAY BE INSERTED ANYWHERE INTERMEDIATE RESULTS ARE DESIRED. THE LAST COMMAND WITHIN THE CIRCUIT DESCRIPTION LOOP WILL NORMALLY BE EITHER "RG" OR "S" TO OBTAIN THE OVERALL RESPONSE. EXAMPLES OF "BLAP" INCLUDING USING THE PLOTTER AND BOTH LINEAR AND LOG FREQUENCY SCALES ARE INCLUDED ALONG WITH THE PROGRAM LISTING TO AID THE USER IN CREATING HIS OWN CIRCUIT DESCRIPTION PROGRAMS.

COMPLEX NUMBER MATHEMATICS IS USUALLY REQUIRED FOR CIRCUIT ANALYSIS (EXCEPT AT DC OR FOR RESISTORS ONLY). "BLAP" CARRIES COMPLEX NUMBERS IN RECTANGULAR FORM FOR ALL OPERATIONS IN ORDER TO ACHIEVE A SPEED IMPROVEMENT OVER USING R-P AND P-R OPERATIONS. THE ROUTINES WITHIN "BLAP" EMPLOY ONLY STACK REGISTERS (X,Y,Z,T,L), R04, AND FLAG 14. "+" AND "-" EVEN SAVE "LAST X+JY" IN THE STACK (Z+JT). THE COMPLEX ARITHMETIC COMMANDS MAY BE EMPLOYED FOR GENERAL USE OUTSIDE OF "BLAP" - JUST REMEMBER THAT "1" USES REGISTER 04; ALL OTHER COMPLEX OPERATIONS AFFECT ONLY THE STACK.

QUICK REFERENCE GUIDE

>AT LEAST TWO MEMORY MODULES ARE REQUIRED<

BLAP COMMANDS:

NAME	DATA FORMAT	FUNCTION PERFORMED
RL	RL	INITIALIZE LOAD RESISTANCE
RG	RG	COMPUTE GAIN FOR RG GEN.
S	RG	COMPUTE SF AND SI FOR RL/RG
Z	(USE R17	COMPUTE IMPEDANCE
VP	AS INDEX	COMPUTE VOLTAGE TO GROUND
IS	MARKER)	COMPUTE SERIES CURRENT

BLAP ELEMENTS:

NAME	DATA FORMAT	FUNCTION PERFORMED
BG	R0 ↗ GDB	REVERSE GAIN BLOCK
GB	R0 ↗ GDB	TRANSISTOR GAIN BLOCK
TL	R0 ↗ Θ0 ↗ F0	TRANSMISSION LINE
TF	N1 ↗ N2	IDEAL TRANSFORMER
PRXS	R ↗ L ↗ C	PARALLEL RLC IN SERIES
PRXP	R ↗ L ↗ C	PARALLEL RLC IN PARALLEL
SRXP	R ↗ L ↗ C	SERIES RLC IN PARALLEL
SRXS	R ↗ L ↗ C	SERIES RLC IN SERIES
PLCS	L ↗ C	PARALLEL LC IN SERIES
PLCP	L ↗ C	PARALLEL LC IN PARALLEL
SLCP	L ↗ C	SERIES LC IN PARALLEL
SLCS	L ↗ C	SERIES LC IN SERIES
PRCS	R ↗ C	PARALLEL RC IN SERIES
PRCP	R ↗ C	PARALLEL RC IN PARALLEL
SRCP	R ↗ C	SERIES RC IN PARALLEL
SRCS	R ↗ C	SERIES RC IN SERIES
PRLS	R ↗ L	PARALLEL RL IN SERIES
PRLP	R ↗ L	PARALLEL RL IN PARALLEL
SRLP	R ↗ L	SERIES RL IN PARALLEL
SRLS	R ↗ L	SERIES RL IN SERIES
RP	R OHMS	R IN PARALLEL
RS	R	R IN SERIES
LP	L NH	L IN PARALLEL
LS	L	L IN SERIES
CP	C PF	C IN PARALLEL
CS	C	C IN SERIES
ZP	R ↗ X	R+JX IN PARALLEL
ZS	R ↗ X	R+JX IN SERIES
OSTP	R0 ↗ Θ0 ↗ F0	OPEN STUB IN PARALLEL
OSTS	R0 ↗ Θ0 ↗ F0	OPEN STUB IN SERIES
SSTP	R0 ↗ Θ0 ↗ F0	SHORTED STUB IN PARALLEL
SSTS	R0 ↗ Θ0 ↗ F0	SHORTED STUB IN SERIES

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COMPLEX MATH OPERATOR       OPERATION PERFORMED
                      1     X+JY=1/(X+JY)
                      /     X+JY=(Z+JT)/(X+JY)
                      *     X+JY=(X+JY)*(Z+JT)
< "LAST X+JY"   >     +     X+JY=(X+JY)+(Z+JT)
< SAVED IN Z+JT >     -     X+JY=(Z+JT)-(X+JY)

REGISTER USE:(MIN SIZE 020, DEG MODE, F00-04 CLEAR)
 00   PLOTTER YMAX           10 PLOTTER XINC
 01   PLOTTER YMIN           11 PLOT "NAME"
 02   PLOT NNN.AAA          >12 RE(V)
 03   PLOT CHARACTER        >13 IM(V)
<04   SCRATCH REGISTER      >14 RE(I)
 05   PLOTTER "FIX" N       >15 IM(I)
 06   PLOTTER FREQUENCY     >16 RL
 07   PLOTTER "X UNITS"     >17 INDEX SYMBOL
<08   FREQUENCY GHZ         >18 SCRATCH REGISTER
 09   PLOTTER XMAX          >19 SCRATCH REGISTER
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001>LBL "BLAP"
002 PPC 3948
003 PROMPT
004>LBL "RL"
005 STO 16
006 STO 12
007 1
008 STO 14
009 0
010 STO 13
011 STO 15
012 FIX 3
013 "F="
014 ARCL 08
015 "⊢ GmZ"
016 AVIEW
017 FIX 2
018 RTN
019>LBL "BG"
020 SF 00
021>LBL "GB"
022 20
023 /
024 10↗ X
025 2
026 /
027 ENTER↗
028 X↗ 2
029 LAST X
030 ST+ X
031 +
032 1
033 +
034 SQRT
035 +
036 ST/ Z
037 ST/ T
038 *
039 STO 04
040 FC?C 00
041 GTO 00
042 RCL 13
043 RCL 12
044 R↗
045 ST/ Z
046 /
047 GTO 01
048>LBL 00
049 -
050 ST/ 12
051 ST/ 13
052 /
053 ST* 14
054 ST* 15
055 RCL 13
056 RCL 12
057 R↗
058 ST* 12
059 ST* 13
060 RDN
061>LBL 01
062 RCL 15
063 RCL 04
064 *
065 ST+ 13
066 RDN
067 RCL 14
068 RCL 04
069 *
070 ST+ 12
071 RDN
072 GTO 05
073>LBL "TL"
074 /
075 RCL 08
076 *
077 1
078 P-R
079 RDN
080 STO 04
081 X<>Y
082 ST/ 04
083 *
084 STO L
085 R↗
086 RCL 13
087 RCL 12
088 RCL 15
089 R↗
090 ST* 12
091 ST* 13
092 ST* 15
093 X<> 14
094 ST* 14
095 X<> L
096 ST* L
097 ST* Y
098 RDN
099 ST- 12
100 RDN
101 LAST X
102 ST+ 13
103 RDN
104 RCL 04
105 ST* Z
106 *
107 X<>Y
108 CHS
109 GTO 05
110>LBL "TF"
111 /
112 ST* 12
113 ST* 13
114 ST/ 14
115 ST/ 15
116 RTN
117>LBL "PRXS
118 SF 04
119 GTO 03
120>LBL "PRXP"
121 SF 04
122>LBL "SRXP"
123 SF 00
124>LBL "SRXS"
125>LBL 00
126 SF01
127 GTO 00
128>LBL "PLCS"
129 SF 04
130 GTO 00
131>LBL "PLCP"
132 SF 04
133>LBL "SLCP"
134 SF00
135>LBL "SLCS"
136>LBL 00
137 SF 03
138 SF 02
139 GTO 07
140>LBL "PRCS"
141 SF 04
142 GTO 00
143>LBL "PRCP"
144 SF 04
145>LBL "SRCP"
146 SF 00
147>LBL "SRCS"
148>LBL 00
149 ENTER↗
150 SF 01
151 SF 03
152 GTO 07
153>LBL "PRLS"
154 SF 04
155 GTO 00
156>LBL "PRLP"
157 SF 04
158>LBL "SRLP"
159 SF 00
160>LBL "SRLS"
161>LBL 00
162 ENTER↗
163 SF 01
164 SF 02
165 GTO 07
166>LBL "RP"
167 SF 00
168>LBL "RS"
169 ENTER↗
170 ENTER↗
171 SF 01
172 GTO 07
173>LBL "LP"
174 SF 00
175 LBL "LS"
176 ENTER↗
177 SF 02
178 GTO 07
179>LBL "CP"
180 SF 00
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181>LBL "CS"
182 SF 03
183>LBL 07
184 STO 04
185 RDN
186 PI
187 ST+ X
188 RCL 08
189 *
190 *
191 LAST X
192 -1 E3
193 /
194 RCL 04
195 *
196 FC?C 03
197 CLX
198 X#0?
199 1/X
200 XEQ 01
201 X<>Y
202 FC?C 02
203 CLX
204 XEQ 01
205 +
206 X<>Y
207 FC?C 01
208 CLX
209 XEQ 01
210 FS? 04
211 CHS
212 GTO 00
213>LBL 01
214 FC? 04
215 RTN
216 X#0?
217 1/X
218 CHS
219 RTN
220>LBL "ZP"
221 SF 00
222>LBL "ZS"
223 X<>Y
224 GTO 00
225>LBL "OSTP"
226 SF 00
227>LBL "OSTS"
228 SF 04
229 GTO 01
230>LBL "SSTP"
231 SF 00
232>LBL "SSTS"
233>LBL 01
234 /
235 RCL 08
236 *
237 TAN
238 X<>Y
239 FS? 04
240 1/X
241 *
242 0
243>LBL 00
244 FS?C 00
245 GTO 00
246 FS?C 04
247 XEQ "1"
248 RCL 15
249 RCL 14
250 XEQ "*"
251 ST+ 12
252 RDN
253 ST+ 13
254 RTN
255>LBL 00
256 FC?C 04
257 XEQ "1"
258 RCL 13
259 RCL 12
260 XEQ "*"
261>LBL 05
262 ST+ 14
263 RDN
264 ST+ 15
265 RTN
266>LBL "S"
267 SF 00
268>LBL "RG"
269 STO 04
270 RCL 15
271 RCL 14
272 RCL 04
273 ST* Z
274 *
275 RCL 13
276 RCL 12
277 XEQ "+"
278 STO 16
279 X<>Y
280 STO 19
281 X<>Y
282 RCL 04
283 RCL 16
284 *
285 SQRT
286 ST+ X
287 ST/ Z
288 /
289 XEQ "1"
290 "G"
291 FS? 00
292 "SF"
293 XEQ 00
294 FC?C 00
295 RTN
296 RCL 13
297 RCL 12
298 2
299 ST* Z
300 *
301 RCL 19
302 RCL 18
303 XEQ "-"
304 RDN
305 RDN
306 XEQ "/"
307 "SI"
308>LBL 00
309 "⊢DB"
310 R-P
311 LOG
312 20
313 *
314 GTO 01
315>LBL "Z"
316 RCL 13
317 RCL 12
318 RCL 15
319 RCL 14
320 XEQ "/"
321 "Z"
322 GTO 00
323>LBL "VP"
324 RCL 13
325 RCL 12
326 "V"
327 GTO 00
328>LBL "IS"
329 RCL 15
330 RCL 14
331 "I"
332>LBL 00
333 FIX 0
334 CF 29
335 ARCL 17
336 FIX 2
337 SF 29
338 R-P
339>LBL 01
340 RND
341 X<>Y
342 RND
343 X<>Y
344 "⊢="
345 ARCL X
346 "⊢<"
347 ARCL Y
348 AVIEW
349 RTN
350>LBL "/"
351 SF 14
352>LBL "1"
353 STO 04
354 X↗ 2
355 RDN
356 CHS
357 X↗ 2
358 ST+ T
359 X<>L
360 R↗
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361 ST/ 04
362 /
363 RCL 04
364 FC?C 14
365 RTN
366>LBL "*"
367 STO L
368 R↗
369 ST* L
370 R↗
371 ST* Z
372 R↗
373 ST* Z
374 ST* Y
375 X<>L
376 +
377 X<>T
378 RDN
379 -
380 RTN
381>LBL "+"
382 ST+ Z
383 RDN
384 ST+Z
385 RDN
386 RTN
387>LBL "-"
388 ST- Z
389 RDN
390 ST- Z
391 RDN
392 END  844 BYTES
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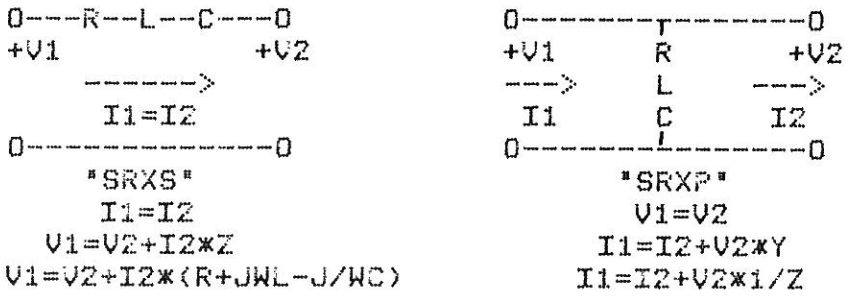
APPENDIX

THE DERIVATION OF SOME OF THE "BLAP" ELEMENT SUBROUTINES IS PRESENTED IN THIS SECTION TO AID THE USER IN CREATING CUSTOMIZED SUBROUTINES FOR HIS NEEDS. FAMILIARITY WITH CIRCUIT ANALYSIS AND WITH USING THE HP-41C ARE THE ONLY PREREQUISITES.

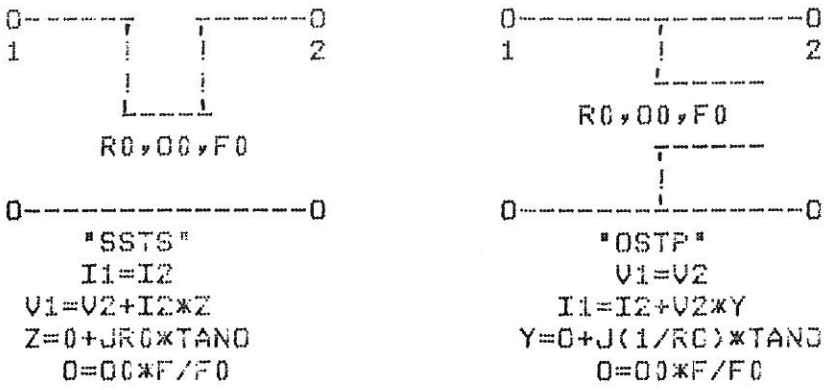
SERIES-PARALLEL RLC'S



EITHER THE IMPEDANCE OF A SERIES RLC OR THE ADMITTANCE OF A PARALLEL RLC IS COMPUTED. "Z<>Y" TRANSFORMATION -IF NECESSARY- IS PERFORMED USING THE "1" COMMAND. FLAG 04 IS USED TO DISTINGUISH BETWEEN SERIES OR PARALLEL RLC CONNECTION WITHIN THE ELEMENT -F04 IS SET IF THE FIRST LETTER OF THE "NAME" IS "P" -. FLAG 00 IS USED TO DISTINGUISH BETWEEN SERIES OR PARALLEL USAGE OF THE ELEMENT WITHIN THE LADDER NETWORK -F00 IS SET IF THE LAST LETTER OF THE ELEMENT "NAME" IS "P" -. F01,F02, AND F03 ARE SET IF RESPECTIVELY R,L, OR C ARE PRESENT WITHIN THE BLOCK. THE FLAGS ARE TESTED LATER TO REMOVE ANY UNUSED ELEMENTS FROM THE GENERAL RLC ELEMENT. IF FLAGS 00 AND 04 MATCH, THE ELEMENT IS USED AS IS, OTHERWISE THE "1" COMMAND CONVERTS Z<>Y.

STUBS

TRANSMISSION LINE STUBS MAY ALSO SIMPLY BE REPRESENTED AS IMPEDANCES OR ADMITTANCES. THE SHORTED STUB IS REPRESENTED AS AN IMPEDANCE, WHILE THE OPEN STUB IS REPRESENTED AS AN ADMITTANCE.

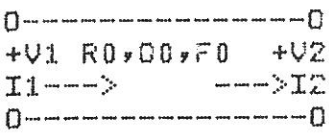


THE ONLY DIFFERENCE BETWEEN THE SHORTED STUB IMPEDANCE -Z- AND THE OPEN STUB ADMITTANCE -Y- IS R0 VERSUS 1/R0. FLAG 04 IS SET FOR AN OPEN STUB -FIRST LETTER "O" AND FLAG 00 IS SET FOR PARALLEL STUB USAGE - LAST LETTER "P". ONCE THE STUB IMPEDANCE OR ADMITTANCE IS DETERMINED THE ELEMENT IS HANDED WITHIN "BLAP" JUST LIKE A LUMPED IMPEDANCE OR ADMITTANCE.

ALMOST ANY PASSIVE FILTER MAY BE ANALYZED USING ONLY THE IMPEDANCE/ADMITTANCE ELEMENTS DESCRIBED ABOVE. "BLAP" DOES NOT PROVIDE ALL POSSIBLE RLC COMBINATIONS; HOWEVER, AND ALSO THE USER MIGHT FIND IT CONVENIENT AND FASTER TO CREATE COMBINATIONS OF EXISTING ELEMENTS. TWO EXAMPLES WHICH MIGHT WARRENT THEIR OWN COMMANDS ARE A QUARTZ CRYSTAL -SERIES RLC WITH A CAPACITOR IN PARALLEL- AND A REAL COIL OR RESISTOR -SERIES RL IN PARALLEL WITH A CAPACITOR. THESE ELEMENTS MAY BE REALIZED USING NORMAL "BLAP" COMMANDS ONLY IF THEY ARE USED AS PARALLEL ELEMENTS.

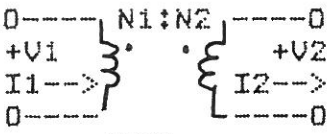
TWO-PORT ELEMENTS

ALL OF THE ELEMENTS DESRIBED SO FAR HAVE EITHER IDENTICAL VOLTAGE ON EITHER SIDE -PARALLEL ELEMENT- OR IDENTICAL CURRENT ON EITHER SIDE -SERIES ELEMENT. MANY VERY USEFUL ELEMENTS MODIFY BOTH THE CURRENT AND VOLTAGE AND MUST BE CONSIDERED AS TWO-PORT NETWORKS -IN FACT THE ELEMENTS DESCRIBED ABOVE ARE SPECIAL TRIVIAL CASES OF TWO-PORT NETWORKS-. THE INPUT/OUTPUT RELATIONSHIP OF A TWO-PORT CAN BE DESCRIBED IN MANY EQUIVALENT WAYS - Z,Y,G,H,S,ABCD - DEPENDING UPON THE CHOICE FROM I1,V1,I2,V2 OF THE PAIRS OF INDEPENDENT AND DEPENDENT VARIABLE PAIRS. IN "BLAP" I2, AND V2 ARE THE INDEPENDENT VARIABLES SO WE ARE REALLY USING "BACKWARDS" ABCD PARAMETERS. THE FOUR TWO-PORTS USED IN "BLAP" ARE PRESENTED BELOW:



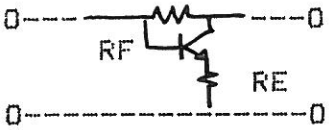
"TL"

I1=I2*COSΘ+JV2*(1/R0)*SINΘ
V1=V2*COSΘ+JI2*R0*SINΘ
Θ=Θ0*F/F0



"TF"

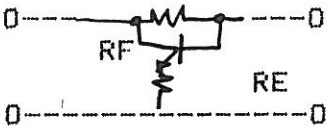
I1=I2*N2/N1
V1=V2*N1/N2
N1, N2 +/-



"GB"

$$V1=\frac{(RE*RF*I2+RE*V2)}{RE-RF}$$

$$I1=\frac{(RE*I2+V2)}{RE-RF}$$



"BG"

V1=RF*I2+V2
I1=I2+V2/RE

R0=SQRT(RF*RE)
S21=(RE-RF)/(RE+R0)
GDB=20*LOG(S21)

THE TWO-PORTS INCLUDED ARE ALL "IDEAL" ELEMENTS. THE TRANSMISSION LINE AND TRANSFORMER ARE LOSSLESS AND THE GAIN BLOCK IS BUILT USING AN IDEAL TRANSISTOR SUCH THAT THE AMPLIFIER PERFORMANCE IS SOLELY DETERMINED BY THE FEEDBACK RESISTORS. THE GAIN BLOCK HAS 180 DEGREES PHASE SHIFT AND IS A PERFECT MATCH IN A R0 OHM SYSTEM. "BLAP" ACTUALLY "DESIGNS" EACH GAIN BLOCK - COMPUTES RF AND RE FOR SPECIFED DB GAIN AND SYSTEM RESISTANCE R0-. SIMULTANEOUS PERFECT MATCH WITH THE GAIN BLOCK IS ONLY POSSIBLE IF THE GENERATOR AND LOAD IMPEDANCES ARE EQUAL. THE "GB" MAY ALWAYS BE CASCADED WITH A TRANSFORMER OR MATCHING NETWORK TO OBTAIN ANY COMBINATION OF SOURCE AND LOAD IMPEDANCES. THE GAIN BLOCK IS UNCONDITIONALLY STABLE SINCE THE INPUT AND OUTPUT MATCH IS PERFECT IN A R0 OHM SYSTEM AND THE REVERSE ISOLATION IS GREATER THAN THE FORWARD GAIN.

CANDIDATES FOR OTHER TWO-PORT ELEMENTS ARE LIMITLESS. LOSSY TRANSMISSION LINE, NON-IDEAL TRANSFORMERS, AND GAIN BLOCKS HAVING "REAL" TRANSISTORS ARE OBVIOUS EXAMPLES. HAPPY PROGRAMMING!